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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,853	11/09/2001	Glen Wada	042390P7196D	4202

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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	11

DATE MAILED: 02/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No	Applicant(s)	
10/052,853	WADA ET AL.	
Examiner	**Art Unit**	
Jack Chen	2813	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 28 January 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: *None*.

   Claim(s) objected to: *None*.

   Claim(s) rejected: *9-15*.

   Claim(s) withdrawn from consideration: *None*.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☒ Other: *See Continuation Sheet*

Continuation of 10. Other: The Examiner maintains previous Office Action dated on 11/25/2002. With respect to objection to the drawings and 35 U.S.C. 112, first paragraph rejection, applicant argues that since the passivation layer 103 covering the substrate 101, which includes flash memory cells, accordingly, the passivation layer 103 covers the flash memory cells. The Examiner disagrees because neither the specification nor the drawings show this particular step. Furthermore, the substrate includes flash memory cell does NOT necessary mean it is formed under the passivation layer. It is also noted that ony a part of the passivation layer is covering the substrate as shown in fig. 1. Applicant further states page, 6, line 3 to page 7, line 2 confirms that passivation layer 103 covers the flash memory cells, the Examiner disagrees because this particular feature is not found at the above cited page, the cited page only described the material for the passivation layer. Furthermore, Kiyoshiko shows using the same material for the passivation layer, i.e, silicon nitride film 9 and polyimide film 10 (fig. 1, which is UV opaque passivation layer), which is the same as appliicant's claimed invention. With respect to 35 U.S.C. 102 (b) rejection, applicant argues that "EPROM" is NOT a "flash memory" the Examiner disagrees because applicant clearly stated on page 2, lines 13-14 "flash memory devices (i.e., Erasable Programmable Read Only Memoried that may be erased electrically)", which is EPROM. Further in this regard, the Examiner would like to point out that the basis text book by Peter Van Zant "Microchip Fabrication" page 550, which states "Flash memories. Flash memories are a form of EEPROM. it is a one transistor cell design, like an EPROM". Applicant further argues the the prior art (Kiyohiko, JP/04-078173) does not show the passivation layer covers its memory cells, the examiner disagrees because fig. 1 clearly shows this feature (passivation layer 9 and 10, and in abstract section, lines 11-13 clearly states "it is not necessary to provide the window 11 to each EPROM element" and the abstract section clearly states that the passivation layer is opaque to UV). Applicant further states "although part of the passivation layer 103 is subsequently removed to form bond pads, those skilled in the art would appreciate that this step will not expose the underlying flash memory cells" in page 4 of the remark section, this is similar to the prior art (fig. 1).

JACK CHEN
PATENT EXAMINER

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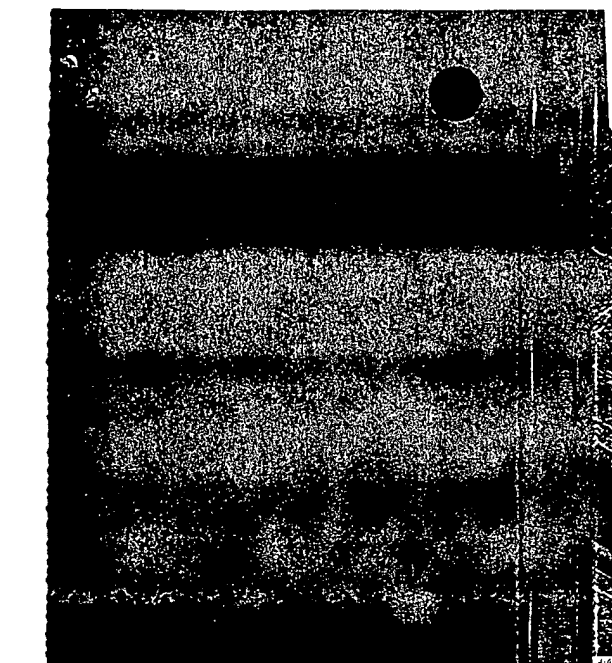

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PETER VAN ZANT

ming machine. A typical EPROM can be reprogrammed up to ten times.

EEPROM. The next level of convenience in memory design is the ability to program and reprogram the chip while it is in a socket in the machine. This convenience is available with the EEPROM (or E^2PROM), standing for electronically erasable PROM. Programming and erasing take place by pulses from the outside that place charges in selected memory cells or drain the charges away. Programming is by the same mechanism used for EPROMs, hot electron infection. Charge is drawn from the memory cell be a mechanism called Fowler-Nordheim tunneling. This connivance comes at the expense of a larger memory cell size and a commensurate reduction in chip density.

Flash memories. Flash memories are a form of EEPROM. It is a one transistor cell design,[1] like an EPROM but has the convenience of in-socket programming and erasure. Additionally blocks, or the entire array, can be erased at one time.

Volatile memories. Semiconductor circuit and computer design involves the constant evaluation of trade-offs. In the case of memory, nonvolatile memory provides protection against power loss, but these memories are frequently slow and not very dense. More importantly, none of the circuits described above has a write capability, an essential feature in operating a computer. New information, such as a change in pay status, must be conveniently entered into the computer and stored temporarily while the new check is being written. Memory must also be easily erasable so the computer can quickly process new information or accept a completely new program. There are several memory circuit designs used to produce fast and high-density memory circuits. Both are of the volatile type; that is, when power is lost to the chip, all the stored information is lost; information presented on a computer screen, and not saved, is eligible for loss if the power to the computer goes off.

RAM. One type of circuit used for high-density memory (Fig. 17.8) storage is random-access memory, or RAM. "Random" refers to the ability of the computer to directly retrieve any information stored in the circuit. Unlike a serial memory, the RAM design allows the chip to find the exact information asked for wherever it is located in the

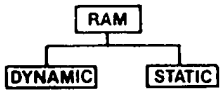

Figure 17.8 RAM cell designs.